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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/277,328 03/26/99 KNEISSL

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EXAMINER

SCHILLINGER, L

ART UNIT

PAPER NUMBER

2813

DATE MAILED:

03/07/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/277,328

Applicant(s)

Knelssl et al

Examiner

Laura Schillinger

Group Art Unit

2813



☒ Responsive to communication(s) filed on Mar 26, 1999

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-13 is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-13 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

2. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Bowers et al ('687).

In reference to claim 1, Bowers teaches a method comprising the steps of:

providing a semiconductor membrane having an insulating substrate (Abs. Lines: 1-5);
attached on a first side of the semiconductor membrane (Abs. Lines: 1-5);
attaching a thermally conducting substrate to a second side of the membrane (Col.4, lines: 5-25);;
removing the insulating substrate from the first side of the semiconductor membrane (Col.4, lines: 10-15);; and
placing a metal layer on the first side of the membrane (Col.7, lines: 40-50);.

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In reference to claim 2, Bowers teaches wherein the substrate is sapphire (Abs, lines: 1-5).

In reference to claim 3, Bowers teaches wherein the step of attaching includes putting a solder layer on the substrate (Col.4, lines: 8-15).

In reference to claim 4, Bowers teaches wherein the solder is selected from the group of In, PbSn and AuSn (Col.4, lines: 8-15).

In reference to claim 5, Bowers teaches wherein the step of removing includes exposing the substrate to a laser (Col.4, lines: 45-50).

In reference to claim 6, Bowers teaches wherein the step of removing includes polishing (Col.5, lines: 5-25).

In reference to claim 7, Bowers teaches wherein the membrane comprises In, Ga, Al and N (Col.4, lines: 8-15).

In reference to claim 8, Bowers teaches wherein the substrate consists of Si (Col.6, lines: 40-45).

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In reference to claim 9, Bowers teaches a method comprising:

providing a semiconductor membrane having a first crystal plane, the membrane having an insulating substrate attached on a first side of the semiconductor membrane and having a plurality of electrodes attached to a second side of the membrane (Abs. Lines: 1-5);

attaching a thermally conducting substrate having a second crystal plane to a first side of the semiconductor membrane such that the first and second planes are aligned (Col.4, lines: 5-25 and Fig.1);

removing the insulating substrate from the first side of the semiconductor membrane (Col.4, lines: 10-15);

placing a metal layer on the first side of the semiconductor membrane (Col.7, lines: 40-50);

In reference to claim 10, Bowers teaches further comprising:

cleaving the substrate along the second crystal plane and the first plane to make facets in the laser diode array (Abs, lines: 10-15).

In reference to claim 11, Bowers teaches wherein the substrate is Si (Col.6, lines: 40-45).

In reference to claim 12, Bowers teaches wherein the second crystal plane is the 111 plane.

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In reference to claim 13, Bowers teaches a method comprising:

providing a semiconductor membrane having a first crystal plane, the membrane having an insulating substrate attached on a first side of the semiconductor membrane and having a plurality of electrodes attached to a second side of the membrane (Abs. Lines: 1-5);

attaching a thermally conducting substrate having a second crystal plane to the first side of the semiconductor membrane such that the first and second planes are aligned (Col.5, lines: 1-5);

removing the insulating substrate from the first side of the semiconductor membrane (Col.4, lines: 10-15);

placing a metal layer on the first side of the semiconductor membrane (Col.7, lines: 40-50);

etching a trench through the metal layer and semiconductor membrane, dividing the metal and semiconductor into two sections (Col.12, lines: 50-55).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sore et al ('491) and Cheung et al ('795) teach similar methods.

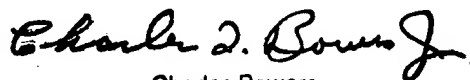
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Any inquiry concerning this communication from examiner should be directed to Laura Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached by telephone on Monday to Friday from 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417. The fax phone number for the group is (703) 308-7722.

LMS

March 2, 2001



Charles Bowers
Supervisory Patent Examiner
Technology Center 2800